

JAPANESE PATENT OFFICE  
PATENT JOURNAL  
KOKAI PATENT APPLICATION NO. HEI 5[1993]-259378

Technical Disclosure Section

Int. Cl. <sup>5</sup> :	H 01 L 27/00 25/065 25/07 25/18 H 01 L 25/08 //H 01 L 21/02 27/15
Sequence Nos. for Office Use:	8418-4M 8934-4M
Application No.:	Hei 4[1992]-52230
Application Date:	March 11, 1992
Publication Date:	October 8, 1993
No. of Claims:	5 (Total of 4 pages)
Examination Request:	Not requested

SEMICONDUCTOR DEVICE

Inventors:	Hidetoshi Matsumoto Hitachi, Ltd. Central Research Laboratory 1-280 Higashi Koigakubo, Kokubunji-shi, Tokyo
------------	---

Tomoki Tanoue  
Hitachi, Ltd. Central  
Research Laboratory 1-280  
Higashi Koigakubo,  
Kokubunji-shi, Tokyo

Hiroshi Masuda  
Hitachi, Ltd. Central  
Research Laboratory  
1-280 Higashi Koigakubo,  
Kokubunji-shi, Tokyo

Applicant:

000005108  
Hitachi, Ltd.  
4-6 Kanda Surugadai,  
Chiyoda-ku, Tokyo

Agent:

Katsuo Ogawa,  
patent attorney

[There are no amendments to this patent.]

#### Abstract

##### Objective

To realize enhanced density at the connecting point when joining and making a compound semiconductor integrated circuit and a Si integrated circuit into one body.

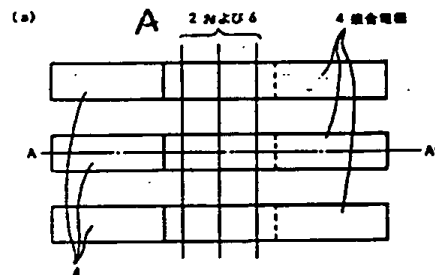
##### Constitution

Groove (2) and semiconductor projection (6) in which the side surface is composed from the (111) surface and are provided

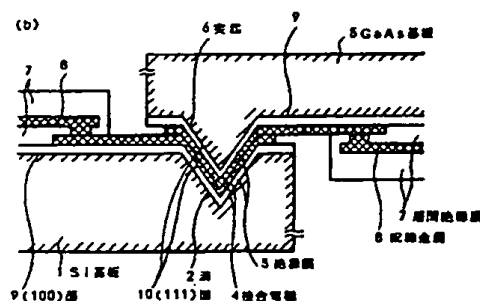
to the connection part of the integrated circuit. Also, junction electrode (4) of metal or alloy thin film is provided on groove (2) and projection (6).

### Effect

The connection part can be refined and enhanced in density by improving the precision in the adhesion and improving the work precision.



Key: A      2 and 6  
          4      Coupling electrode



- Key: 1 Si substrate  
 2 Groove  
 3 Insulating film  
 4 Coupling electrode  
 5 Galts substrate  
 6 Protrusion  
 7 Interlayer insulating film  
 8 Wiring metal  
 9 (100) plane  
 10 (111) plane

### Claims

1. A semiconductor device characterized by the fact that the first semiconductor element or integrated circuit having a semiconductor projection grid aligned with the substrate in which the substrate surface is composed from the (100) surface, and the side surface is composed from the (111) surface, and the second semiconductor element or integrated circuit having a groove engraved in the substrate in which the substrate surface is composed from the (100) surface, and the side surface is composed from the (111) surface have a structure of being joined by mutually opposing the groove and the projection.

2. A semiconductor device in Claim 1, in which the junction part of the groove and the projection are joined via a metal or alloy thin film having electrical connection to the first and second semiconductor elements or integrated circuits.

3. A semiconductor device in Claim 1 or 2, in which the substrate material of said first semiconductor element or said integrated circuit is GaAs or InP or GaP, the substrate material of the second semiconductor element or said integrated circuit is Si, a light-emitting element is included in the first semiconductor element or said integrated circuit, and a light-receiving element is included in the first or second semiconductor element or integrated circuit.

4. A fabrication method for semiconductor device in Claim 1, 2, or 3, in which the semiconductor projection grid aligned with the substrate in which the side surface is composed from the (111) surface and the groove engraved in the substrate in which the side surface is composed from the (111) surface are formed according to selective growth or etching having planar bearing dependency.

5. A system which transmits and receives optical signals between semiconductor devices by optically connecting the light-emitting element and light-receiving element of different semiconductor devices by plurally using said semiconductor device in Claim 3.

\* \* \*